**ECTE432 – Pipelined MIPS Processor**

I designed a pipelined mips processor in Verilog. However, when implementing my design onto simulink, errors occurred that I could not solve. In project ise my pipelined version of a processor simulates correctly and functionality works.

The steps to open and simulate my pipelined mips processor:

1. Open up the file pipeline\_mips.xise by double clicking on it.
2. Click the simulation view in ISE Project Navigator.
3. Click on the file mips\_pipeline\_tb.v .
4. Below expand the ISim Simulator and right click on “Simulate Behavioral Model”.
5. When the ISim wavescope opens up click file open and search for the file PipelinedWavefor.wcfg
6. A pop up message appears click on the “Connect to Existing” button.
7. Click the “Re-Launch” button on the top right of the ISim wavescope.
8. Wait for the ISim wavescope to compile and the simulation waveform appears.
9. You can zoom into the wave scope using the buttons of “ctrl + mouse scroll” or using the Zoom in, Zoom out and or Zoom to full view button in ISim wavescope.

